PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-255442
(43)Date of publication of application : 21.09.1999

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(51)Int.Cl. B66B 1/30
H02P 7/63

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(21)Application number : 10-063236
(22)Date of filing : 13.03.1998
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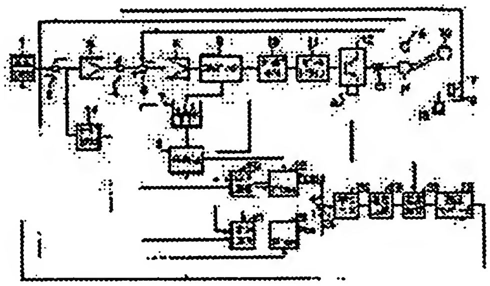
(54) ELEVATOR CONTROL DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce the absolute value of a junction temperature by calculating the switching loss when a semiconductor power element in an inverter device is switched, and calculating the on-loss when the semiconductor power element is turned on and a constant current flows.
SOLUTION: This elevator control device is provided with a switching loss arithmetic unit 20 momentarily receiving the voltage command signal of a comparator 9, the output current signal of a current detector 13, and a proximate polynominal and add-calculating the switching loss of a power element. The elevator control device is also provided with an on-loss arithmetic unit 21 calculating the momentary on-loss based on the voltage command signal, the output current signal, and the proximate polynominal like the switching loss calculation when a semiconductor element such as IGBT is turned on and a current flows in a transistor. Even when a low-frequency large current flows, the momentary IGBT loss and a junction temperature rise are calculated, it is momentarily calculated that the temperature of a chip in the IGBT becomes the guaranteed maximum temperature, and a control current is lowered to prevent the temperature rise.



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LEGAL STATUS
[Date of request for examination] 26.03.2001

[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3350439
[Date of registration]	13.09.2002
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the elevator control unit equipped with the converter equipment which consists of the inverter equipment which consists of a semi-conductor power component or this inverter equipment, and a semi-conductor power component.
[0002]
[Description of the Prior Art] The outline configuration of an example of the elevator control device equipped with the conventional inverter control device is shown in drawing 17 . It is the rectifier which 34 in drawing rectifies a three-phase-alternating-current power source, and 35 rectifies the three-phase-alternating-current power source 34, and is changed into a direct current. They are the smoothing capacitor which carries out smooth [of the DC power supply whose 36 is the output of a rectifier 36], and inverter equipment which 12 uses a smoothing capacitor 36 as DC power supply, and changes into alternating current power by the inverter control of an adjustable electrical-potential-difference variable frequency. 14 is a three-phase induction motor (a motor is called below) driven with inverter equipment 12. 30 is a sheave rotated together through the reducer which it is directly linked with a motor 14 and is not illustrated.
[0003] Moreover, 16 is counter balance weight and this is constituted through the rope by the elevator cage 17 and the ** type to hang to the sheave 30. 37 is a thermostat for laying temperature detection attached in the condensator of the semi-conductor power component (below : power component which is not what is restricted to this is called although expressed with IGBT by a diagram) which constitutes inverter equipment 12.
[0004] As actuation of the outline of such a component, a rectifier 35 rectifies the alternating current of AC power supply 34, and this direct current is stored in a smoothing capacitor 36. When an elevator starts, by supplying energy and driving a motor 14 with inverter equipment 12 from said DC power supply, a sheave 30 rotates and a cage 17 and counter balance weight 16 move in the vertical direction. If operation is continued, power component exoergic loss is accumulated gradually and power component heat sinking plane temperature rises. And if the laying temperature of a thermostat 37 is further reached under the effect of a service condition, ambient temperature, etc., by outputting a detecting signal from a thermostat 37, an elevator is stopped, or nearby story implantation will be carried out and operation of an elevator will once be stopped.
[0005] Moreover, it is set up so that the laying temperature of this thermostat may determine, a junction temperature rise of the chip in a power component at the time of overload max may be specified as a direction and it may become below the maximum temperature that can be power component guaranteed.
[0006] Next, outline explanation is given about the count approach of a junction temperature rise of the above-mentioned chip in a power component. It becomes an operation pattern as shown in drawing 18 as operation of an elevator. 31 in drawing 18 is constituted from a rate pattern outputted from a speed setter (after-mentioned) by the acceleration field A, the stationary transit (rated speed) field B, and the moderation field C. 32 in drawing is the torque command signal which added the cage weighted signal (after-mentioned) to the deflection signal of the output of said speed setter, and the output of a rate detector (after-mentioned), and the magnitude of the output current which flows to a motor 14 according to the magnitude of this electrical potential difference is determined. When

the left-hand side rate of area A is 0, if a frequency becomes high and it results in rated speed on the right-hand side of the acceleration field A, as for the inverter output current 33, the output current will also become rated frequency, as a frequency begins from 0Hz and a rate becomes quick. Also at the time of moderation, similarly, a frequency becomes low gradually and a frequency is set to 0Hz at the time of a halt.

[0007] Moreover, since the counter balance weight 16 and the cage 17 used as the load of a sheave 30 with which, as for the thing with a large current, a motor 14 is directly linked by the stationary travel corridor B in the acceleration field A are also accelerated together, big currents also including those inertial force are needed. Acceleration torque TFLACC If expressed, it will become like (1) type shown below. TFLACC = (GDM 2+GDS 2) k-alpha+TM -- (1)

Here, it is GDM 2.: The moment of inertia of a motor 14, and GDS 2 : An axial conversion factor [in / a sheave or subsequent ones / the moment of inertia of a load (counter balance weight, a cage self-weight, loading), and the hand of cut from k:motor shaft to a sheave 30], alpha: Acceleration, TM : Rating torque in stationary transit.

[0008]

[Problem(s) to be Solved by the Invention] Thus, it is Above TFLACC when accelerating an elevator cage. In order to give driving torque to a motor, it is necessary to pass a big current to rating, and when a rate is low, in order to perform variable frequency control further and to pass the current of a low frequency, the burden to the power component in inverter equipment 12 becomes large.

[0009] Since the frequency changes every moment as count of a junction temperature rise of the chip in a power component in case the current of the above-mentioned low frequency high current flows for a power component, If loss is calculated on the basis of this frequency, it will become indefinite, for example, loss will be calculated by the maximum current in the frequency of nearly 0Hz, in order to search for loss by the almost direct-current-count as control frequency, It becomes large as mean loss, and if it is going to hold down the junction temperature in the mean loss to below the maximum temperature that can be guaranteed, it is necessary to suppress low the temperature rise of the cooling fin at the time of stationary loss, and will become large-sized as a cooling system.

[0010] Moreover, if loss is calculated by the maximum current in a frequency when comparatively high, since it will become the loss 1/pi Carried out and will be calculated more smallish to the loss at the time of a direct current as mean loss, at the time of actual low frequency high current energization, there is whenever [no / allowances], junction temperature may exceed the maximum temperature which can be guaranteed depending on the case, and a power component may be damaged by the thermal run away.

[0011] Furthermore, since the loss searched for at the time of low-frequency high-current energization since only average loss was searched for from the loss which changes in an instant instant since the actual current is changing in the shape of a sine wave with the period decided by the frequency from 0A to maximum current lacked accuracy and was not able to judge it in a large value and a small value to actual loss, it had become what took a margin quite thermally at the time of the design of a condensator.

[0012] Although it indicated above and also the intelligent power component (IPM) which detects the chip temperature of IGBT has appeared on the market in the commercial scene recently Since the transitional temperature rise of the junction section cannot be followed in detection by the above-mentioned detector, When using it in an elevator, the momentary temperature rise in the field A of drawing 17 is undetectable, exceeding the maximum temperature which can be guaranteed is considered enough and it has not become a perfect detection function to the chip side junction temperature in IGBT.

[0013] This invention can control a junction temperature rise of the power component which constitutes power converters, such as inverter equipment, and aims at offering the elevator control unit which can prevent **** by the thermal run away of the chip in a power component.

[0014]

[Means for Solving the Problem] In order to attain said purpose, invention corresponding to claim 1 In the elevator control unit which has inverter equipment which carries out drive control of the AC motor which operates an elevator cage in the vertical direction The switching loss computing element which calculates a momentary switching loss in case said semi-conductor power component in inverter equipment switches, Elevator control unit ****** equipped with the on-loss computing element which calculates a momentary on-loss when said semi-conductor power component turns on and the fixed current is flowing.

[0015] According to invention corresponding to claim 1, it becomes possible by presuming a momentary junction temperature rise from a switching loss and an on-loss to mitigate the load to said power component according to junction temperature.

[0016] In order to attain said purpose, invention corresponding to claim 2 The inverter equipment which carries out drive control of the AC motor which operates an elevator cage in the vertical direction, The speed regulating device which forms the rate detector which detects the rotational speed of said motor, and performs rate minor-loop control, The current control unit which forms the current detector which detects the current which flows to said motor, and performs current minor-loop control, The equipment and the setting device which generate the triangular wave signal for performing PWM control, The armature-voltage control equipment which carries out the party rate of the output signal and triangular wave signal of said current control device, and creates the DETTO time of a signal further, In the elevator control device which has gate drive equipment which supplies the signal of said armature-voltage control equipment to each semi-conductor power component of inverter equipment A current in case said semi-conductor power component in inverter equipment switches, and the relation of loss are expressed more than to the primary approximate polynomial. The output signal from a current detector, and the switching loss computing element which calculates a momentary switching loss from said approximate polynomial, Said semi-conductor power component turns on and a current when the fixed current is flowing, and the relation of the main circuit saturation voltage between power components are expressed more than with the primary approximate polynomial. The signal signal from said current detector, and the on-loss computing element which calculates a momentary on-loss from said approximate polynomial, The output signal of said switching loss computing element, and the average switching loss computing element which calculates the average of a switching loss based on the frequency from said setting device, The output signal of said on-loss computing element, and the average stationary on-loss computing element which calculates the average of an on-loss based on the inverter output frequency detected from said rate detector, Per [which adds the output signal of said average switching loss computing element and an average stationary on-loss computing element, and calculates the average loss per chip in a semi-conductor power component] chip, an average loss computing element, It is the elevator control unit equipped with said chip, transient thermal resistance of a heat sinking plane, and chip junction temperature rise adder that adds the junction temperature rise with a chip from the average loss computing-element output per said chip.

[0017] According to invention corresponding to claim 2, the following operations are acquired. Loss of the power component to the momentary current of **** when the current is flowing in the shape of a sine wave at the time of the low frequency high current energization at the time of acceleration and deceleration characteristic at the time of elevator operation sometimes A switching loss, By calculating according to an individual by the on-loss, and calculating the junction temperature rise in the instant Since the temperature of the heat sinking plane of a power component condensator is added and the absolute value of the power component chip junction temperature in an instant is known, Acceleration is lowered, current maximum is reduced or an elevator is stopped [**** / lowering a carrier frequency in an instant if it results in the maximum temperature which can be power component guaranteed]. Power component chip junction temperature always in the place below the pair cost temperature which can be guaranteed Inverter control and converter control can be performed now.

[0018] In order to attain said purpose, invention corresponding to claim 3 The thermometric element in which the temperature detection to linearity, such as a thermistor attached in the heat sinking plane of a condensator in which the semi-conductor power component of said inverter equipment is attached in the elevator control device according to claim 2, is possible, Said junction temperature adder output is inputted as the junction temperature adder adding said chip junction temperature rise adder output and said thermometric element output, and it has a junction temperature comparator in comparison with the maximum temperature of a semi-conductor power component which can be guaranteed.

[0019] Invention corresponding to [in order to attain said purpose] claim 4 is the elevator control device constituted so that the acceleration or deceleration of an elevator speed setter included in said speed regulating device might be lowered and a setting change might be made when it detected that said junction temperature comparator operated in the elevator control device according to claim 3, and junction temperature is over the maximum temperature which can be guaranteed.
[0020] In order to attain said purpose, invention corresponding to claim 5 Said junction temperature comparator operates in an elevator control device according to claim 3. When it detects that junction temperature is over the maximum temperature which can be guaranteed, When the elevator is operating in acceleration mode, a setup of the elevator speed setter contained in said speed regulating device from the moment of detecting is made into moderation mode from acceleration mode. Or it is the elevator control unit which apply electromagnetic brake and it is made to make stop to said motor, a reboot is applied after fixed time amount progress or the temperature output of said thermometric element becomes below the fixed set point, and continued elevator operation.
[0021] In order to attain said purpose, invention corresponding to claim 6 It has the power running and the regeneration mode detector which detects that it is in power running and a regeneration mode condition in an elevator control device according to claim 2 according to the polarity of the deflection signal of the output of the elevator speed setter contained in said speed regulating device, and the output of said rate detector. When said power running and regeneration mode detector detect power running mode Only the section in which the ON signal of said gate drive equipment is contained in said on-loss computing element calculates an on-loss. When said power running and regeneration mode detector detect regeneration mode, only the section containing the off signal of said gate drive equipment is the elevator control unit which calculated the on-loss.
[0022] In order to attain said purpose, invention corresponding to claim 7 An on-loss is calculated for every fixed operation period during the section when the ON signal is contained in gate drive equipment in the elevator control device according to claim 2 as the operation approach when carrying out the digital operation of the operation of said on-loss computing element in the case of power running mode. When the on-loss calculated for every period is added and the ON signal was completed until an ON signal was completed, it is the elevator control unit it was made to output from an on-loss computing element as a total-on loss in the ON signal at that time.
[0023] In order to attain said purpose, invention corresponding to claim 8 In an elevator control unit according to claim 2, as an approach when calculating the operation of an on-loss computing element by the analogue device The multiplier of the main circuit electrical potential difference of said semiconductor device in case a detection current and its current flow an analogue device in the case of power running mode, While constituting from an integrator which integrates with said multiplier output, carrying out initiation of a multiplier and the integrator of operation with the pulse edge of the ON signal included in said gate drive equipment, stopping the above-mentioned integral control action by the pulse edge of an off signal and applying a clearance It is the elevator control unit which was made to consider output voltage with which it has integrated till then to said on-loss computing element as the output.
[0024] In order to attain said purpose, invention corresponding to claim 9 As opposed to the detection current at the time of an ON signal or an off signal going into said gate drive equipment as the operation approach of said switching loss computing element in an elevator control device according to claim 2 It is the elevator control unit calculates and adds the switching-on with the value of the instantaneous detection current, and a switching off loss to coincidence, and it was made to output the result of an operation from said switching loss computing element as a switching loss in one on-pulse.
[0025] In order to attain said purpose, invention corresponding to claim 10 As opposed to the detection current at the time of an ON signal going into a gate drive signal from said gate drive equipment as the operation approach of said switching loss computing element in an elevator control device according to claim 2 As opposed to the detection current in the time of calculating the switching-on loss in the value of the detection current in the moment, and an off signal going into a gate drive signal It is the elevator control unit adds the switching-on loss and switching off loss which calculated the switching off loss in the value of the detection current in the moment, and were calculated by said separate time amount, and it was made to output from said switching loss

computing element as a switching loss.
[0026] In order to attain said purpose, invention corresponding to claim 11 In an elevator control device according to claim 2 to the input side of said inverter equipment The converter equipment which changes the alternating current of AC power supply into a direct current is connected. Said switching loss computing element, said on-loss computing element, said average switching loss computing element, It is the elevator control unit which added said average stationary on-loss computing element and the junction temperature rise arithmetic unit which consists of an average loss computing element and said chip junction temperature rise adder per said chip.
[0027] In order to attain said purpose, invention corresponding to claim 12 It considers as the configuration which attached in the heat sinking plane the laying temperature detector which will be detected in an elevator control unit according to claim 2 or 3 if it results in the laying temperature of a thermostat etc. instead of thermometric elements, such as said thermistor. It is the elevator control unit which adds the laying temperature to said junction temperature adder during the period which said laying temperature detector detected, and which has been detected at the time [a period], and calculated junction temperature.
[0028] In order to attain said purpose, invention corresponding to claim 13 is the elevator control device which supervised whether a package of equipment which calculates junction temperature only to a part for the plane 1 of said AC motor would be prepared, and junction temperature would be over the maximum temperature which can be guaranteed in an elevator control device according to claim 2 or 3.
[0029] In order to attain said purpose, invention corresponding to claim 14 is the elevator control device which supervised whether a package of equipment which calculates junction temperature to all the two phases or three phase circuits of said AC motor would be prepared, and junction temperature would be over the maximum temperature which can be guaranteed in an elevator control device according to claim 2 or 3.
[0030] In order to attain said purpose, invention corresponding to claim 15 In the elevator equipment which has attached thermometric elements, such as a thermistor, in the condensator which has mass inverter equipment which constitutes a condensator according to an individual for every phase with the elevator control device according to claim 2 or 3 It is the elevator control unit which inputs into the junction temperature adder which indicated the value which had the comparator which measures the output of each phase thermometric element, and has detected the maximum temperature of a thermometric element by claim 3, and calculated the junction temperature only for a plane 1 among those for a three phase circuit.
[0031] the elevator equipment which had mass inverter equipment which invention corresponding to claim 16 is an elevator control device according to claim 2 or 3, and constitutes a condensator according to an individual for every phase in order to attain said purpose, and has attached thermometric elements, such as a thermistor, in each condensator -- setting -- the output of each phase thermometric element -- a part for a three phase circuit -- the junction temperature adder formed separately -- inputting -- each phase -- it is the elevator control device which calculated junction temperature individually.
[0032] [0033] which according to invention according to claim 3 to 16 can control a junction temperature rise of the power component which constitutes power converters, such as inverter equipment, and can prevent **** by the thermal run away of the chip in a power component
[Embodiment of the Invention] < -- operation gestalt [of ** a 1st]: -- to claim 1, correspondence > drawing 1 is the block diagram showing the 1st operation gestalt, gives the same sign to the same part as drawing 17 , and omits the explanation.
[0034] The output of the elevator speed setter which generates the elevator rate pattern 31 which explained one by drawing 18 among drawing, and the rate detector 15 with which 2 detects the rate of a motor 14, The rate adder which adds the output of the elevator speed setter 1 by the minor loop, The rate computing element which 3 inputs the deflection of said rate adder 2, and adjusts the rate response of proportionality, an integral, differential, oscillating control, etc., The weighted signal adder adding the detecting signal of the load detector 18 with which 4 detects the load of the elevator cage 17, and the output of said rate computing element 3, The current adder which adds the output of the current detector 3 with which 5 detects the output current of inverter equipment 12, and the

output of said weighted signal adder 4 by the minor loop, The current computing element which 6 inputs the deflection signal of said current adder, and adjusts the current response of proportionality, an integral, etc., The triangular wave generator for generating a triangular wave for 7 carrying out PWM control, The triangular wave setter to which 8 sets the amplitude and period (frequency) of said triangular wave generator 7, The comparator which 9 inputs the output of said triangular wave generator 7 and current computing element 6, and creates an electrical-potential-difference command signal, The dead-time amendment machine which sets up the DETTO time of the top arm of inverter equipment 12 and a bottom arm to the electrical-potential-difference command signal with which 10 becomes the output of said comparator 9, and 11 are gate drive equipment which creates the signal which drives each power component of inverter equipment 12. The equipment of a sign explained above is conventionally constituted also in equipment.

[0035] As this operation gestalt, the component added newly is described below. The switching loss computing element which 20 inputs the signal of an electrical-potential-difference command and the output of the current detector 13 which are an output of a comparator 9, and calculates the switching loss of a power component, 21 inputs a current signal and an electrical-potential-difference command signal like the switching loss computing element 20. The on-loss computing element which calculates an on-loss when the current is flowing, and 22 input the output of the signalling frequency of a triangular wave wave from the triangular wave setter 8, and said switching loss computing element 20 into a power component. The average switching loss computing element which calculates the average of a switching loss based on the carrier frequency of a triangular wave signal, The average stationary on-loss computing element which calculates the average of an on-loss based on the inverter output frequency to which 23 was outputted from the speed signal of the rate detector 15, The power component switching-on loss adder which 24 adds the output of said average switching loss computing element 22 and the average stationary on-loss computing element 23, and outputs momentary power component generating loss, 25 per [which inputs the output of said power component switching-on loss adder 24, and calculates the generating loss per chip in an instant] chip An average loss computing element, 26 is a chip junction temperature rise adder adding the junction temperature of the instant instant while it inputs the output of the average loss computing element 25 per said chip and converts the momentary generating loss into a junction temperature rise within a chip.

[0036] In addition, it has the thermistor 27 needed with the operation gestalt later mentioned in addition to the configuration described above, the junction temperature adder 28, and the junction temperature comparator 29.

[0037] Next, actuation of the 1st operation gestalt constituted as mentioned above is explained. sign 1in drawing - since 18 and 30 are conventionally the same as that of the configuration in an elevator, they carry out an explanation abbreviation about these actuation. First, actuation of the switching computing element 20 and the operation approach are explained. It is the current IC </SUB> which flows for a power component as shows power components, such as IGBT, to drawing 2 to the gate drive conditions which generally exist. It has the property of Loss mj. They are loss in case an axis of abscissa shows the current which flows to the main circuit transistor of IGBT, and expresses the loss at the time of the switching to each current value to an axis of ordinate in drawing 2 and Eon carries out switching-on, and Eoff. It is loss when carrying out switching-off.

[0038] First, this property is expressed more than with the primary polynomial, and the relational expression of the loss over the current which flows to IGBT is defined. For example, if it assumes that it expresses with the 3rd polynomial, they are Eon and Eoff as follows. It is expressed.

[0039]

Eon=aIC 3+bIC 2+cIC+d (2) Eoff =eIC 3+fIC 2+gIC+h -- here -- IC : Constant when expressing with the 3rd polynomial the rated current and the property of a-h: drawing 2 of flowing to IGBT.

[0040] Therefore, the signal by the pulse of the electrical-potential-difference command by the output of a comparator 9 is Eon in the instantaneous carrying current, and Eoff by reading the instantaneous carrying current at that time by making the time of a pulse edge in case IGBT turns on entering into trigger conditions. It is determined more nearly uniquely than (2) types. Then, Eon and Eoff which were determined A switching loss when said trigger conditions enter calculates by adding. And if the following IGBT on-pulse enters as shown in drawing 3 , the instantaneous carrying current in the moment will be read again, and they are new Eon and Eoff. It becomes the configuration of calculating. Above Eon and Eoff It is Ptsw about an addition signal. It is [0041] when it carries out.

[Equation 1]

$$P_{tsw} = \sum_{n=1}^{n} (E_{oni} + E_{offi}) \text{ (mj)} \quad \cdots (3)$$

When it switches to one period of ******** and the inverter control current n times, a switching loss is added like (3) types.

[0042] Next, the average switching loss computing element 22 is explained. It is the momentary switching loss Ptsw by carrying out the multiplication of the frequency of a triangular wave to the signal outputted with the switching loss computing element 20. It receives and is the average switching loss Psw (W). It calculates.

[0043] Moreover, if the current which flows to IGBT only in one arm (for example, U phase) of inverter equipment 12 is indicated as shown in drawing 4 , when the P side IGBT38 turns on the current shown as the continuous line of a sine wave when sinusoidal current as shown in drawing flows for U phase load terminal, it will flow, but since the current shown with the broken line of a sine wave flows to the N side IGBT39, it will not flow to the P side IGBT38. Therefore, an average switching loss of as opposed to [since loss occurs in IGBT by the half cycle to one period of a sine wave] the P side IGBT38 is set to one half, and is Psw (w). If a formula shows, it will become like (4) types.

[0044]

thereforePsw=Ptsw xfC x1/2 (w) -- (4)

Average switching loss fC of the moment the Psw:IGBT on-pulse entered : A triangular wave carrier frequency, next the on-loss computing element 21 are explained. Semiconductor devices, such as IGBT, have a current as shown in drawing 5 , and the property of an electrical potential difference, while it turns on and the current is flowing to the transistor. It is the saturation voltage VCE between collector emitters of a transistor [as opposed to / the current to which an axis of abscissa flows to the main circuit transistor of IGBT in drawing 5 is shown, and / each current value to an axis of ordinate] (sat). It expresses. Therefore, VCE to the current which expresses the property of drawing 5 more than with the primary polynomial, and flows to IGBT like the time of a switching loss operation also here (sat) Relational expression is defined. For example, when it assumes that it expresses with the 3rd polynomial, it is expressed as follows.

[0045]

VCE(sat) (V) =kIC 3+lIC 2+mIC+n -- (5)

The constant when expressing the property of k-h: drawing 5 with the 3rd polynomial here. Therefore, the signal by the pulse of the electrical-potential-difference command by the output of a comparator 9 is VCE (sat) in the instantaneous carrying current by making the time of a pulse edge in case IGBT turns on entering into trigger conditions, and reading the instantaneous carrying current at that time. It is determined more nearly uniquely than (5) types.

[0046] And it is deltat (s) after the above-mentioned on-pulse edge enters. Supposing an off pulse enters behind, it is the deltat (s). On-loss Pton of a between It is expressed as follows.

Pton(J) =deltatxVCE (sat) xIC -- (6)

(When the magnitude between [IC] deltat does not change)

Or when currents when a current and an off-pulse when an on-pulse enters enter differ, trapezoid approximation is carried out like drawing 6 , and it is deltat (s). The on-loss which can be set is calculated as follows.

[0047]

P1 ton=VCE(sat) 1xIC1 P2 ton=VCE(sat) 2xIC2 -- (7)

thereforePton(J) =deltatx (P1 ton+P2ton)/2 -- it calculates by (6) and one of (7) types as mentioned above, and considers as the output signal of the on-loss computing element 21.

[0048] Next, the average stationary on-loss computing element 23 is explained. It is the average stationary on-loss Pon (W) by carrying out the multiplication of the frequency f of the inverter control current detected from the speed signal of the rate detector 15 to the output signal of said on-loss computing element 21. It is calculated as follows.

[0049]
Pon (W) =Pton xf -- (8)
(8) The value calculated by the formula is outputted from the average stationary on-loss computing element 23. And the total loss PLOSS of IGBT in one switching operation until the IGBT ON signal shown by the pulse train of drawing 3 enters and the following ON signal enters calculates by adding the average switching-on loss and average stationary on-loss which were calculated by (4) types and (8) formulas with the IGBT switching-on loss adder 24.
[0050] And in consideration of the current imbalance during the chip in IGBT etc., the chip loss Q to the worst chips, such as current imbalance, is further calculated as follows to said total loss PLOSS, and it outputs from the average loss computing element 25 per chip.
[0051]
Q (W) =AxPLOSS/N -- (9)
The chip total constituted in N:IGBT, such as current imbalance within A:chip, here.
[0052] It inputs, whenever IGBT switches total loss, and he carries out sequential addition of the junction temperature rise at that time, and is trying to output to the heat network containing the thermal resistance Pth (fc) which finally exists in a chip-heat sinking plane to the total loss Q generated for the chip, the heat capacity Cigbt of an IGBT chip, etc. from the chip junction temperature rise adder 26.
[0053] Thus, since the junction temperature rise can be calculated, calculating the IGBT loss to the current of an instant instant to the low frequency current generated in the shape of a sine wave, it can calculate correctly to a junction temperature rise.
[0054] By according to the 1st operation gestalt described above, calculating the IGBT loss and the junction temperature rise in an instant instant, even when a low frequency high current like the field A of drawing 18 flows It calculates could guarantee the junction temperature of the chip in IGBT and having become the maximum temperature in an instant. The control current can be lowered, or a carrier frequency can be lowered, or an elevator can be stopped, the increment in loss can be prevented so that junction temperature may not rise any more, and breakage by the thermal run away of the chip in an IGBT power component can be prevented.
< -- operation gestalt [of ** a 2nd]: -- claim 2 -- correspondence > -- the 2nd operation gestalt is an elevator based on the signal of the IGBT chip junction temperature rise shown in drawing 1, and describes the approach of protecting for the junction temperature.
[0055] In drawing 1, the thermometric element in which temperature detection is possible, and 28 to linearity, such as a thermistor which attached 27 in the heat sinking plane in [IGBT] inverter equipment, the chip junction temperature rise adder 26, The junction temperature adder which inputs the output of said thermometric element 27 and calculates the absolute value of chip junction temperature, 29 inputs the output of said junction temperature adder 28, and compares with the maximum temperature which is guaranteed as IGBT, which is junction temperature and which can be guaranteed. The output of the comparator 9 is inputted into the triangular wave setter 8 with the junction temperature comparator which outputs a detecting signal when the output beyond said maximum temperature is inputted.
[0056] Moreover, drawing 7 shows the example of a concrete circuit into which the triangular wave carrier frequency is changed, when the above-mentioned junction temperature comparator is outputted. As for a pull-up resistor and 41, in drawing 7, 40 is [a NAND gate and 42] the inverter gates. Moreover, 43 and 44 are circuits which carry out the operation after current control by digital control by gate array ** DSP when packing into one IC the equipment to 6-10 of a sign shown by drawing 1 (digital signal processor).
[0057] Next, actuation of this operation gestalt is explained with reference to drawing 1 and drawing 7. If the loss which will be generated from IGBT if an elevator is operated continuously serves as heat with a radiation fin and the temperature of a cooling fin rises, the output of the thermometric element 27 attached in the heat sinking plane of a cooling fin becomes high. The output of this thermometric element 27 and the output of the chip junction temperature rise adder 26 are inputted into the junction temperature adder 28, and it is junction temperature absolute value deltatj of chip max. It calculates as follows.
[0058]

deltatj =ta+tigbt -- (10)
Here, it is ta. : The output signal of a thermometric element, tigbt: Output signal of a chip junction temperature rise adder.
[0059] this deltatj it inputs into the following junction temperature comparator 29 -- having -- the maximum temperature Tj which can be guaranteed exceeding (Tj <deltatj) -- the signal of "H" is outputted as an output of a comparator 29. Moreover, the output of a comparator 29 will be inputted into the place of 29 of drawing 7 . It sets to drawing 7 and is 43 gate arrayf1. When a terminal is "H", the triangular wave carrier frequency of f1 is set up within GA, and it is f2. When a terminal becomes "H", it is f2 within GA. It is set as a triangular wave carrier frequency. Since another ["L" and / its] input is always "H" by the pull-up resistor 40 among the inputs of NAND gate 41 in the signal of a comparator 29 when the comparator 29 has not detected, the output of NAND gate 41 serves as "H", and it is f1. A terminal is "H" and f2. The terminal is "L" and is the usual triangular wave carrier frequency f1. It is controlled.
[0060] However, it is f1, when a comparator 29 detects, the output becomes "H", the output of NAND gate 41 is set to "L" and the output of the inverter gate 42 serves as "H". A terminal is "L" and f2. A terminal serves as "H" and a triangular wave carrier frequency is f2. A setting change is made. f1 and f2 It is relation f1 >f2 By carrying out, a comparator 29 detects and chip junction temperature is Tj <deltatj. If it becomes relation, it will become possible to lower a triangular wave carrier frequency. That this triangular wave carrier frequency falls is fC shown by (4) formulas. By meaning falling and making the average switching loss Psw small after all, the average loss Q falls per chip, a junction temperature rise is suppressed, and it is junction temperature deltatj absolutely. It can lower.
[0061] Thus, it is deltatj by lowering a triangular wave carrier frequency and suppressing loss from the moment the comparator 29 detected. Absolute temperature can be controlled. In addition, even if the circuit of drawing 7 uses analogue devices, such as an operational amplifier, it is realizable.
[0062] < -- operation gestalt [of ** a 3rd]: -- claim 3 -- correspondence > -- although the 3rd operation gestalt is explained with reference to drawing 1 , by approaches other than the triangular wave carrier frequency explained with the 2nd operation gestalt, it is the approach of lowering junction absolute temperature, and this is explained below.
[0063] It is Tj <deltatj with the junction temperature comparator 29 in drawing 1 . Although the method of detecting relation is the same as the 2nd operation gestalt, the output is inputted into an elevator speed setter here.
[0064] The actuation in this case is explained with reference to drawing 8 . When the elevator rate pattern 31 tends to issue an acceleration command and an elevator tends to accelerate, supposing a comparator 29 outputs "H" in the place where the time amount of D passed, it is an acceleration setup from the time alpha 1 of the present condition alpha 2 shown with a broken line The output current of acceleration is controlled and it is made to lower a junction temperature rise by changing.
[0065] acceleration -- alpha 1 from -- alpha 2 Acceleration torque TFLACC shown by (1) formula when it changes Since it falls, acceleration current peak value falls, the switching loss Psw and the on-loss Pon are reduced, and a junction temperature absolute value can be controlled.
[0066] < -- operation gestalt [of ** a 4th]: -- claim 4 -- correspondence > -- although the 4th operation gestalt was made with the same configuration as the 3rd operation gestalt, it was made for differing from the 3rd operation gestalt to make moderation mode just stop [time / of a comparator 29 detecting the rate pattern from the elevator speed setter 1] a change elevator on a nearby story from acceleration mode
[0067] Actuation of the 4th operation gestalt of such a configuration is explained with reference to drawing 9 . When it is [rate-pattern] under acceleration and a comparator 29 detects at the time of F hour progress, you switch to moderation mode (G) from acceleration mode, and make it implanted on a nearby story in a speed setter 1 in drawing 9 (a) from the time. Although F period is passed to the IGBT transistor side like a continuous line as a current which flows to IGBT to that by the side of [IGBT38] the U phase P, the comparator 29 of the loss over the chip by the side of a transistor is lost by becoming regeneration mode and coming to flow to the FWD side of IGBT like a broken line, in order for after detection to change to a moderation pattern, and junction temperature can be lowered.

[0068] moreover, the 4th operation gestalt -- it is, and since the output current stops zero and IGBT switching operation from the moment of detecting about the approach of applying brakes, naturally a junction temperature absolute value can be lowered.

[0069] < -- operation gestalt [of ** a 5th]: -- claim 5 -- correspondence > -- about the operation of the on-loss Pon indicated with the 1st operation gestalt, a point which is the same configuration mostly and is different from the operation gestalt which shows the 5th operation gestalt to drawing 1 is the operation approach in power running and regeneration mode, and indicates this below. It is the power running and the regeneration mode detector which 19 in drawing 1 inputs the output of a speed setter 1 and the rate detector 15, inputs the output of the rate adder 2 which outputs a deflection signal, and detects power running and regeneration mode, and the output of the mode detector 19 is inputted into the on-loss computing element 21.

[0070] Drawing 10 explains the operation approach in this operation gestalt. When it detects that power running and the regeneration mode detector 19 are in power running mode, it becomes as shown in drawing 10 (a), (b), and (c). That is, to the U phase P side IGBT38, it is IU. The continuous line of a current flows to the sense of an arrow head, and it is Current IU to IGBT39. A broken line flows to the sense of an arrow head.

[0071] For example, if the current of a continuous line is explained, an IGBT current will flow [the output of a comparator 9] to the transistor side of IGBT38 to the triangular wave output of the triangular wave generator 7, and the output (ignition signal by the side of [IGBT38] the U phase P) of the comparator 9 outputted through the comparator 9 in the current command value of the current computing element 6 at the time of ON [heights with the wide pulse width of drawing 10 (c)].

[0072] Moreover, a current flows [the output of a comparator 9] to FWD by the side of [IGBT39] the V phase N at the time of OFF [heights with the narrow pulse width of drawing 10 (c)]. Therefore, since the ON section of the output of a comparator 9 and IGBT ON become together in this case, an on-loss while the output of a comparator 9 turns on is calculated.

[0073] Furthermore, when power running and the regeneration mode detector 19 detect regeneration mode, it becomes like drawing 10 (d), (e), and (f). That is, to IGBT38, it is IU. The broken line of a current flows to the sense of an arrow head, and it is IU to IGBT39. The continuous line of a current flows to the sense of an arrow head. For example, if the current of a broken line is explained, (the ignition signal of IGBT39) will turn into a reversal signal to the output (ignition signal of IGBT38) of a comparator 9. When the ignition signal of this IGBT39 is an ON command, an IGBT current flows to the transistor side of IGBT39 [heights with the wide pulse width of drawing 10 (f)]. Moreover, when the ignition signal of IGBT39 is an OFF command, a current flows to FWD of IGBT38 [heights with the narrow pulse width of drawing 10 (f)].

[0074] When the output of a comparator 9 turns this off to the output of a comparator 9, a current will flow to IGBT39. Therefore, since it becomes the off section of the output of a comparator 9, and the timing that IGBT ON is together in the case of regeneration mode, an on-loss when the output of a comparator 9 turns off is calculated.

[0075] thus, one signal of the output of a comparator 9 -- trigger conditions -- carrying out -- power running and regeneration -- also in any, an on-loss can be calculated correctly.

< -- operation gestalt [of ** a 6th]: -- claim 6 -- correspondence > -- although the configuration of the 6th operation gestalt is almost the same as that of drawing 1, a different point is the operation approach of an on-loss, and is explained with reference to drawing 11 about this. When calculating an on-loss by digital control, since an operation period becomes discrete, a continuous on-loss operation cannot be performed. Therefore, as shown in drawing 11, it is made to carry out the operation period of an on-loss to every deltat, and the total loss Pton over the on-pulse in the output of a comparator 9 (J) is calculated by adding the on-loss calculated each operation period. The operation approach in the mode of drawing 11 is shown below using (6) types.

[0076]

[Equation 2]

$$P_{t1}=P_{t2}=P_{t3}=P_{t4}=P_{t5}=P_{t6}=P_{t7}=\Delta t \times V_{CE(sat)} \times I_{C1}$$

$$P_{ton(J)}=\sum_{n=1}^{7} P_{tn}$$

[0077] The on-loss operation by the digital control by this operation approach can also be calculated comparatively correctly.
< -- operation gestalt [of ** a 7th]: -- claim 7 -- correspondence > -- although the configuration of the 7th operation gestalt is almost the same as that of drawing 1 , a different point is the operation approach of an on-loss, and is explained with reference to drawing 12 about this below. The operation approach of an on-loss is an approach of calculating an on-loss by the analog circuit unlike the 6th operation gestalt. 49 is analog switches, such as FET into which 45 in drawing performs 46 and the inverter gate and 52 input an analog signal, the pull down resistor by which 48 is connected to 0V, the pull down resistor by which 47 and 56 are connected to the negative electrical potential difference VEE, and an IC like drawing 5 . As for the function generator which outputs the relation of VCE, the multiplier with which 50 calculates an instant on-loss, and 51, the input resistance of an operational amplifier 55 and 53 are discharge resistance of a capacitor 54.
[0078] Actuation of the circuit of this drawing 12 is explained. If the output of a comparator 9 serves as "H" now, an analog switch 46 turns on and an analog switch 52 is turned off. VCE shown by drawing 5 by inputting the signal of the current detector 13 into a function generator 49 when an analog switch 46 turns on (sat) An electrical potential difference is outputted. This VCE (sat) The signal of an electrical potential difference and the current detector 13 is inputted into a multiplier 50, and it is Pt =IC xVCE (sat). It calculates and is Pt. It calculates and is Pt. It is outputted.
[0079] This Pt The function and integral which input and turn on the signal in the integrating circuit constituted from 51, 54, and 55 are continued. And when an analog switch 46 turns off, the signal from the current detector 13 will be lost, and if the output of a comparator 9 becomes off, an integral will be stopped, when it is set to 0V and the output of a multiplier 50 is set to 0. Since an analog switch 52 turns on in this and coincidence, the charge charged by the capacitor 54 discharges through the discharge resistance 53, and the output of an operational amplifier 55 is cleared. Since the output of a multiplier 50 will also change together in connection with it if the output current of the current detector 13 changes while finding the integral, an exact on-loss operation can be performed.
[0080] < -- operation gestalt [of ** an 8th]: -- claim 8 -- correspondence > -- although the configuration of the 8th operation gestalt is almost the same as that of drawing 1 , a different point is the switching loss operation approach, and is explained with reference to drawing 3 about this below.

[0081] The output of a comparator 9 reads the current value of the moment of issuing an ON command, calculates Eon1 and Eoff1 to coincidence based on the current value, and asks for the switching loss Ptsw1 to the on-pulse by Ptsw =Eon1+Eoff1. No operation is performed when the output of a comparator 9 turns off. Next, if an on-pulse enters, it will ask for the new switching loss Ptsw2 by Ptsw2=Eon2+Eoff2 again. Simplification of an operation can be attained by doing in this way.
[0082] < -- operation gestalt [of ** a 9th]: -- claim 9 -- correspondence > -- although the configuration of the 9th operation gestalt is almost the same as that of drawing 1 , a different point is the switching loss operation approach, and is explained with reference to drawing 13 about this below.
[0083] Although the current actually outputted from inverter equipment 12 is based also on the inductance by the side of a load, it is fluctuating every only like drawing 13 . Therefore, the output of a comparator 9 falls, to a current when dirty, the output of a comparator 9 starts the switching-on loss Eon again, and a switching off loss is calculated to a current when dirty here. It is as follows from (2) types as operation expression.
[0084] Eon1 =aI1 3+bI1 2+cI1+dEoff1=eI2 3+fI2 2+gI2+hEon2 =aI3 3+bI3 2+cI3+dEoff2=eI4 3+fI4 2+gI4+h -- thereby Eon and Eoff The result of an operation becomes exact and can calculate an accurate switching loss.
[0085] < -- operation gestalt [of ** a 10th]: -- claim 10 -- correspondence > -- in an elevator control device, the 10th operation gestalt is the pressure up used, regeneration, and converter equipment which performs fixed armature-voltage control, and forms the junction temperature rise arithmetic unit of the inverter equipment explained to the power component like IGBT with the above-mentioned operation gestalt, for example which constitutes converter equipment.

[0086] This is specifically a configuration shown in drawing 17 . Instead of a rectifier 35 There are a pressure up, regeneration, and converter equipment that performs fixed armature-voltage control. For the power component of this converter equipment Per the switching loss computing element 20 of drawing 1 , the on-loss computing element 21, the average switching loss computing element 22, the average stationary on-loss computing element 23, the switching-on loss adder 24, and chip, the average loss computing element 25, the chip junction temperature rise adder 26, a thermistor 27, The junction temperature rise arithmetic unit which consists of a junction temperature adder 28 and a junction temperature comparator 29 is formed. Points other than this have the same composition as drawing 1 .

[0087] If it is in the 10th operation gestalt described above, of course, inverter equipment can attain the miniaturization of the improvement equipment of dependability also to converter equipment.
< -- operation gestalt [of ** an 11th]: -- claim 11 -- correspondence > -- the detector to outputs, such as a thermistor, becomes unnecessary by making it a junction temperature absolute value calculate, and the 11th operation gestalt can attain simplification of a circuit, and low cost-ization of the detector itself, only when the setting thermometric element which performs laying temperature detection of a thermostat etc. instead of thermometric elements, such as a thermistor, is formed and detected.

[0088] < -- operation gestalt [of ** a 12th]: -- claim 12 -- correspondence > -- the 12th operation -gestalt will be made to carry out the means which lowers junction temperature to a total phase, if the equipment of the sign of 19-29 shown in drawing 1 is formed only to a part for a plane 1 and chip junction temperature exceeds the maximum temperature which can be guaranteed with the prepared phase. The protection to the junction temperature which this shows by this patent by the easy circuitry only for a plane 1 is attained.

[0089] < -- operation gestalt [of ** a 13th]: -- claim 13 -- correspondence > -- the 13th operation gestalt is shown in drawing 14 . The same sign is given to the same part as drawing 1 in drawing, and the explanation is omitted. Among drawing, 57 is V phase and 58 is a junction temperature arithmetic unit for W phases at the junction temperature arithmetic unit for U phases and this appearance in which 56 contain the component to 20-29 in drawing 1 . They are the detection current 2 phase / three-phase-circuit inverter which changes an output into the current detector 13 with which 59 detects the OR gate and 60 detects the current of two phase among the output currents of inverter equipment 12 at 2 phases / three phase circuit. Actuation of this circuit is explained. If U phase voltage output command is inputted into U phase junction temperature arithmetic unit among the outputs of a comparator 9 and chip junction temperature exceeds the maximum temperature which can be guaranteed, "H" signal will be outputted from 56, if this is inputted into the OR gate 59, the output will serve as "H" and the means which lowers junction temperature as that to which junction temperature exceeded the allowed value will be carried out.

[0090] The same is said of V phase and W phase. Since it is supervised at the time of all homologouses also when the current imbalance by the phase should arise by this, the abnormalities in junction temperature are certainly detectable.

[0091] < -- operation gestalt [of ** 14th]: -- claim 14 -- correspondence > -- the 14th operation gestalt is shown in drawing 15 . As for U phase inverter stack in which 61 in drawing mounted IGBT of U phase arm, and 62, V phase inverter stack and 63 are W phase inverter stacks.

[0092] Moreover, as for the thermometric element for U phases which attached 64 in U phase condensator heat sinking plane, and 65, the thermometric element for V phases and 66 are the thermometric elements for W phases. The maximum signal detecter which 67 inputs the signal of said thermometric element of 64, 65, and 66, and outputs the largest value, and 68 are junction temperature arithmetic units which have the component of 19-29. It inputs into the junction temperature arithmetic unit which chose maximum by 67 to the detection temperature from 64, 65, and 66 as this actuation, and was formed in the phase of one of U-W phases to that maximum detection temperature, and junction temperature is calculated. When there is variation of a condensator which this established separately for every phase, temperature of the condensator with the highest temperature can be used as the base, and junction temperature can be calculated.

[0093] < -- operation gestalt [of ** 15th]: -- claim 15 -- correspondence > -- the 15th operation gestalt is shown in drawing 16 . This is what combined the circuit of drawing 14 and drawing 16 , inputs the output of the thermometric element 64 for U phases into the junction temperature arithmetic unit 56 for V phases to U phase, and calculates junction temperature. The same is said of V phase and W phase. Thereby, the junction temperature by the condensator temperature variation for every phase and current variation can be supervised according to an individual.

[0094]

[Effect of the Invention] By this invention, the transitional junction temperature at the time of the low frequency high current energization at the time of elevator acceleration is received. By asking for the on-loss and switching loss of an instant instant, and calculating the absolute temperature of the junction temperature in an instant by calculating the junction temperature rise in an instant and adding the temperature of an IGBT clamp face further from those total loss When the calculated junction temperature exceeds the maximum temperature which can be guaranteed, lower the carrier frequency of a triangular wave, or lower acceleration, lower an energization current, and it gets down and carries out. Since it can prevent damaging by the thermal run away which becomes possible [reducing a junction temperature absolute value], and is produced with abnormality heating in an IGBT chip, while inverter equipment and dependability become high Since it can be used now to the place in front of IGBT chip temperature to a radiator, it becomes possible to be able to miniaturize the radiator itself and to also realize low cost and a miniaturization.

[Translation done.]

* NOTICES *

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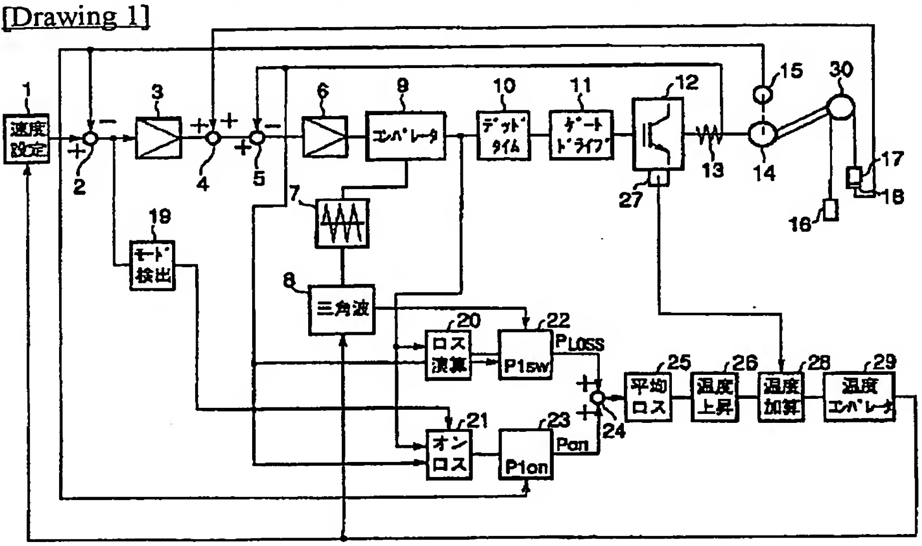
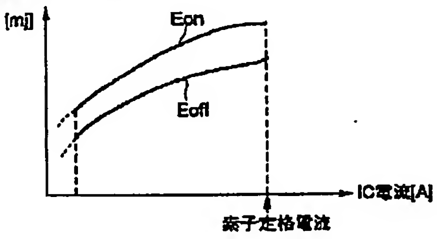
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

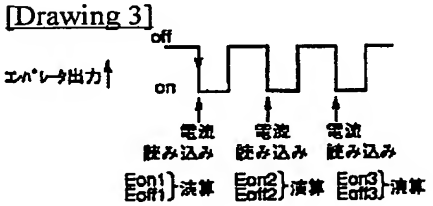
[Drawing 1]


1
速度設定
2
3
4
5
6
9
エンパレータ
10
デッドタイム
11
ゲートドライブ
12
13
14
15
30
17
18
16
27
7
19
モード検出
8
三角波
20
ロス演算
22
P1sw
PLOSS
21
オンロス
23
P1on
Pon
24
25
平均ロス
26
温度上昇
28
温度加算
29
温度エンパレータ

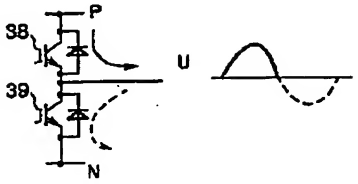
[Drawing 2]



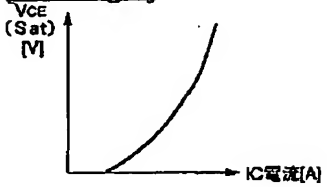
[Drawing 3]


エンパレータ出力
off
on
電流読み込み
電流読み込み
電流読み込み
Eon1 Eoff1 }演算
Eon2 Eoff2 }演算
Eon3 Eoff3 }演算

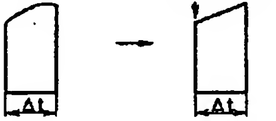
[Drawing 4]



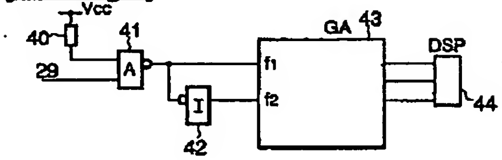
[Drawing 5]



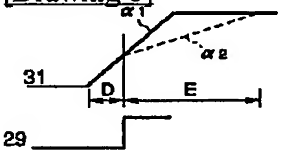
[Drawing 6]


P1 ton
P2ton
At
At

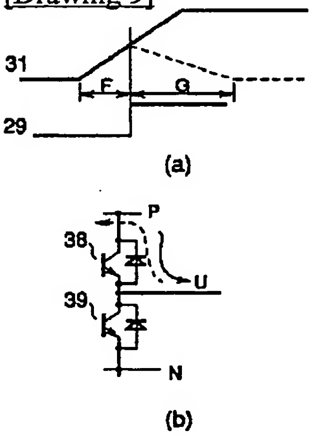
[Drawing 7]


Vcc
40
41
29
A
I
42
GA
43
f1
f2
DSP
44

[Drawing 8]


α1
α2
31
D
E
29

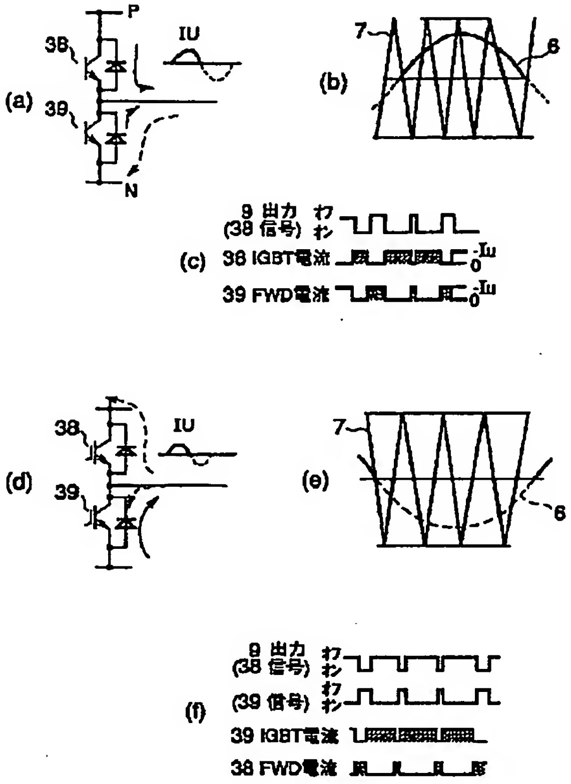
[Drawing 9]


31
F
G
29
P
38
39
U
N

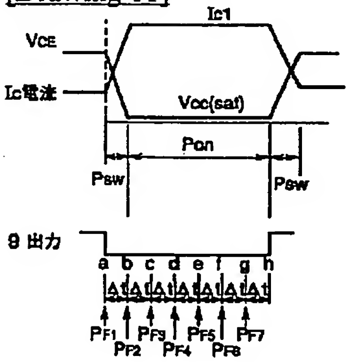
(a)

(b)

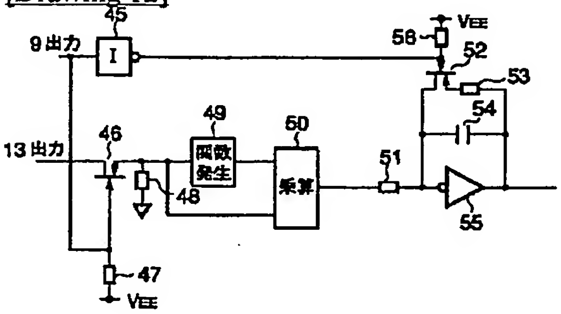
[Drawing 10]


(a)
P
38
39
N
IU
(b)
7
6
(c)
9 出力
(38 信号)
オフ
オン
38 IGBT電流
39 FWD電流
Iu
0
(d)
38
39
IU
(e)
7
6
(f)
9 出力
(38 信号)
(39 信号)
オフ
オン
39 IGBT電流
38 FWD電流

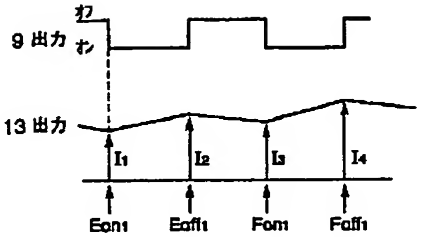
[Drawing 11]


Ic1
VCE
Ic電流
Vce(sat)
Pon
Psw
Psw
9 出力
a b c d e f g h
Δt
PF1
PF2
PF3
PF4
PF5
PF6
PF7

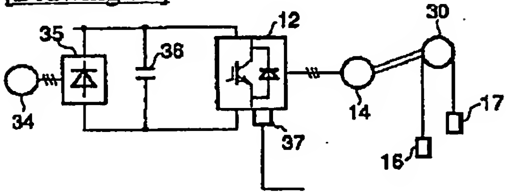
[Drawing 12]


45
I
9 出力
13 出力
46
47
VEE
48
49
関数発生
50
乗算
51
52
53
54
55
56
VEE

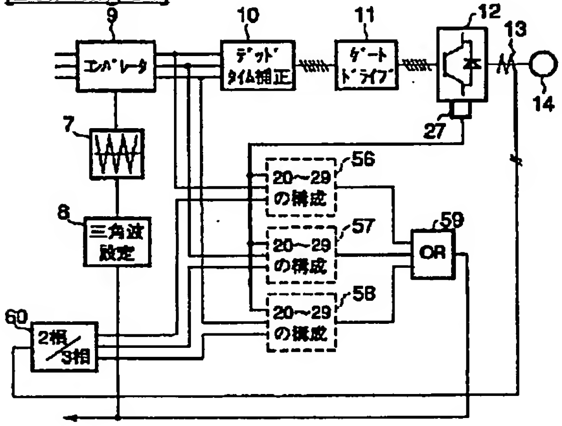
[Drawing 13]



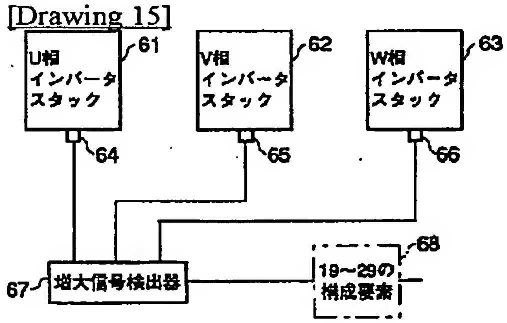
[Drawing 17]


35
36
12
30
34
14
17
37
16

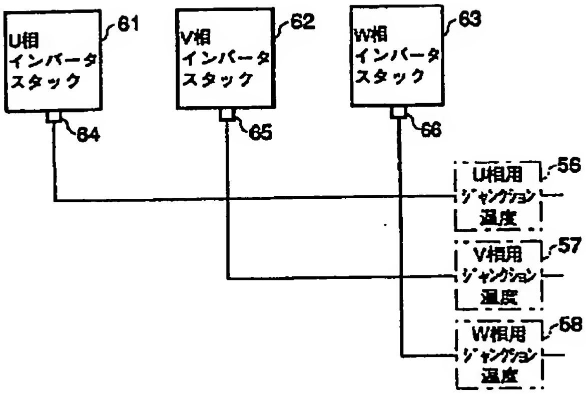
[Drawing 14]


9
10
11
12
13
コンパレータ
デッドタイム補正
ゲートドライブ
14
7
27
56
20～29の構成
57
20～29の構成
59
OR
8
三角波設定
58
20～29の構成
60
2相/3相

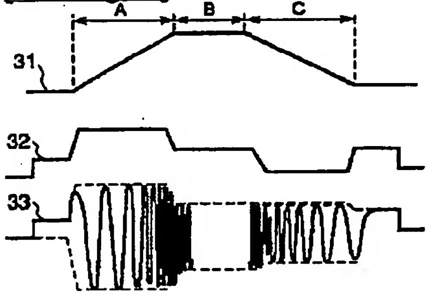
[Drawing 15]


U相インバータスタック
61
V相インバータスタック
62
W相インバータスタック
63
64
65
66
68
67
増大信号検出器
19～29の構成要素

[Drawing 16]


U相
インバータ
スタック
61
V相
インバータ
スタック
62
W相
インバータ
スタック
63
64
65
66
U相用
ジャンクション
温度
56
V相用
ジャンクション
温度
57
W相用
ジャンクション
温度
58

[Drawing 18]



[Translation done.]

* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] In the elevator control unit which has inverter equipment which carries out drive control of the AC motor which operates an elevator cage in the vertical direction The switching loss computing element which calculates a momentary switching loss in case said semi-conductor power component in inverter equipment switches, The on-loss computing element which calculates a momentary on-loss when said semi-conductor power component turns on and the fixed current is flowing, The elevator control unit characterized by presuming a momentary junction temperature rise from a preparation, these switching loss, and an on-loss, and mitigating the load to said power component according to this junction temperature.
[Claim 2] The inverter equipment which carries out drive control of the AC motor which operates an elevator cage in the vertical direction, The speed regulating device which forms the rate detector which detects the rotational speed of said motor, and performs rate minor-loop control, The current control unit which forms the current detector which detects the current which flows to said motor, and performs current minor-loop control, The equipment and the setting device which generate the triangular wave signal for performing PWM control, The armature-voltage control equipment which carries out the party rate of the output signal and triangular wave signal of said current control device, and creates the DETTO time of a signal further, In the elevator control device which has gate drive equipment which supplies the signal of said armature-voltage control equipment to each semi-conductor power component of inverter equipment A current in case said semi-conductor power component in inverter equipment switches, and the relation of loss are expressed more than to the primary approximate polynomial. The output signal from a current detector, and the switching loss computing element which calculates a momentary switching loss from said approximate polynomial, Said semi-conductor power component turns on and a current when the fixed current is flowing, and the relation of the main circuit saturation voltage between power components are expressed more than with the primary approximate polynomial. The signal signal from said current detector, and the on-loss computing element which calculates a momentary on-loss from said approximate polynomial, The output signal of said switching loss computing element, and the average switching loss computing element which calculates the average of a switching loss based on the frequency from said setting device, The output signal of said on-loss computing element, and the average stationary on-loss computing element which calculates the average of an on-loss based on the inverter output frequency detected from said rate detector, Per [which adds the output signal of said average switching loss computing element and an average stationary on-loss computing element, and calculates the average loss per chip in a semi-conductor power component] chip, an average loss computing element, Said chip, transient thermal resistance of a heat sinking plane, and chip junction temperature rise adder that adds the junction temperature rise with a chip from the average loss computing-element output per said chip, A preparation, the elevator control unit characterized by enabling it to presume the momentary junction temperature rise at the time of the low frequency high current control which serves as severe load conditions to said semi-conductor power component.
[Claim 3] The thermometric element in which the temperature detection to linearity, such as a thermistor attached in the heat sinking plane of a condensator in which the semi-conductor power component of said inverter equipment is attached in the elevator control device according to claim 2, is possible, The junction temperature adder adding said chip junction temperature rise adder output

and said thermometric element output, A junction temperature comparator [the maximum temperature of a semi-conductor power component which can be guaranteed / input said junction temperature adder output and], When it detects that it **** and said junction temperature comparator is over the maximum temperature which can be guaranteed, The elevator control unit characterized by reducing a switching loss by making a setting change so that the frequency set point of said setter equipment may be lowered, and making it lower junction temperature.

[Claim 4] The elevator control device characterized by said junction temperature comparator operating, reducing a switching loss and an on-loss by making a setting change in an elevator control device according to claim 3 so that the acceleration or deceleration of an elevator speed setter included in said speed regulating device when it detects that junction temperature is over the maximum temperature which can be guaranteed may be lowered, and making it lower junction temperature.

[Claim 5] Said junction temperature comparator operates in an elevator control device according to claim 3. When it detects that junction temperature is over the maximum temperature which can be guaranteed, When the elevator is operating in acceleration mode, a setup of the elevator speed setter contained in said speed regulating device from the moment of detecting is made into moderation mode from acceleration mode. Or the elevator control unit characterized by applying electromagnetic brake, making it make it stop to said motor, applying a reboot after fixed time amount progress or the temperature output of said thermometric element becomes below the fixed set point, and continuing elevator operation.

[Claim 6] It has the power running and the regeneration mode detector which detects that it is in power running and a regeneration mode condition in an elevator control device according to claim 2 according to the polarity of the deflection signal of the output of the elevator speed setter contained in said speed regulating device, and the output of said rate detector. When said power running and regeneration mode detector detect power running mode Only the section in which the ON signal of said gate drive equipment is contained in said on-loss computing element calculates an on-loss. It is the elevator control unit with which only the section in which the off signal of said gate drive equipment is contained when said power running and regeneration mode detector detect regeneration mode is characterized by calculating an on-loss.

[Claim 7] An on-loss is calculated for every fixed operation period during the section when the ON signal is contained in gate drive equipment in the elevator control device according to claim 2 as the operation approach when carrying out the digital operation of the operation of said on-loss computing element in the case of power running mode. The elevator control unit characterized by making it output from an on-loss computing element as a total-on loss in the ON signal at that time when the on-loss calculated for every period is added and the ON signal was completed until the ON signal was completed.

[Claim 8] In an elevator control unit according to claim 2, as an approach when calculating the operation of an on-loss computing element by the analogue device The multiplier of the main circuit electrical potential difference of said semiconductor device in case a detection current and its current flow an analogue device in the case of power running mode, While constituting from an integrator which integrates with said multiplier output, carrying out initiation of a multiplier and the integrator of operation with the pulse edge of the ON signal included in said gate drive equipment, stopping the above-mentioned integral control action by the pulse edge of an off signal and applying a clearance The elevator control unit characterized by considering output voltage with which it has integrated till then as an output to said on-loss computing element.

[Claim 9] As opposed to the detection current at the time of an ON signal or an off signal going into said gate drive equipment as the operation approach of said switching loss computing element in an elevator control device according to claim 2 The elevator control unit characterized by calculating and adding the switching-on with the value of the instantaneous detection current, and a switching off loss to coincidence, and making it output the result of an operation from said switching loss computing element as a switching loss in one on-pulse.

[Claim 10] As opposed to the detection current at the time of an ON signal going into a gate drive signal from said gate drive equipment as the operation approach of said switching loss computing element in an elevator control device according to claim 2 As opposed to the detection current in the time of calculating the switching-on loss in the value of the detection current in the moment, and an

off signal going into a gate drive signal The switching off loss in the value of the detection current in the moment is calculated. The elevator control unit characterized by adding the switching-on loss and switching off loss which were calculated by said separate time amount, and making it output from said switching loss computing element as a switching loss.
[Claim 11] The elevator control device carry out having connected the converter equipment which changes the alternating current of AC power supply into the input side of said inverter equipment at a direct current in the elevator control device according to claim 2, and having added said switching loss computing element, said on-loss computing element, said average switching loss computing element, said average stationary on-loss computing element, and the junction temperature rise arithmetic unit that becomes per said chip from an average loss computing element and said chip junction temperature rise adder as the description.
[Claim 12] The elevator control unit which considers as the configuration which attached in the heat sinking plane the laying temperature detector which will be detected in an elevator control unit according to claim 2 or 3 if it results in the laying temperature of a thermostat etc. instead of thermometric elements, such as said thermistor, and is characterized by adding the laying temperature to said junction temperature adder during the period which said laying temperature detector detected, and which has been detected at the time [a period], and calculating junction temperature.
[Claim 13] The elevator control device characterized by supervising whether a package of equipment which calculates junction temperature only to a part for the plane 1 of said AC motor was prepared in the elevator control device according to claim 2 or 3, and junction temperature is over the maximum temperature which can be guaranteed.
[Claim 14] The elevator control device characterized by supervising whether a package of equipment which calculates junction temperature to all the two phases or three phase circuits of said AC motor was prepared in the elevator control device according to claim 2 or 3, and junction temperature is over the maximum temperature which can be guaranteed.
[Claim 15] In the elevator equipment which has attached thermometric elements, such as a thermistor, in the condensator which has mass inverter equipment which constitutes a condensator according to an individual for every phase with the elevator control device according to claim 2 or 3 The elevator control unit characterized by inputting into the junction temperature adder which indicated the value which had the comparator which measures the output of each phase thermometric element, and has detected the maximum temperature of a thermometric element by claim 3, and calculating the junction temperature only for a plane 1 among those for a three phase circuit.
[Claim 16] the elevator equipment which had mass inverter equipment which constitutes a condensator according to an individual for every phase, and has attached thermometric elements, such as a thermistor, in each condensator with the elevator control device according to claim 2 or 3 -- setting -- the output of each phase thermometric element -- a part for a three phase circuit -- the junction temperature adder formed separately -- inputting -- each phase -- the elevator control device characterized by calculating junction temperature individually.

[Translation done.]